ABSTRACT OF THE DISCLOSURE

The present invention provides a System-On-Chip (SOC) architecture that utilizes an embedded ferroelectric memory component to store information so that in the event that power is removed from the system, when power returns, the processor of the SOC can resume execution at the point at which it was executing in an instruction set when power was removed. The SOC architecture preferably also includes re-configurable hardware to enable the SOC to be easily re-configured and to have good performance characteristics. The configuration and current execution state of the re-configurable hardware may also be stored in the ferroelectric memory component so that if power cycle occurs, the re-configurable hardware can resume execution at the point at which it was executing when power was lost. The re-configurable hardware may also have its own ferroelectric memory component embedded therein to enable the configuration of the hardware and its current execution state to be stored in the ferroelectric memory component of the re-configurable hardware.